**SABANCI UNIVERSITY
Faculty of Engineering and Natural Sciences**

**Electronics Engineering**: **EE 202 - Electronic Circuits II**
**Spring-2021-2022**

**Instructor:** Prof. Dr. Yaşar Gürbüz

 yasar@sabanciuniv.edu

 Room# 1044 (MDBF)

 Phone# 9533

https://sabanciuniv.zoom.us/j/2554580251

https://sabanciuniv.zoom.us/my/yasar.gurbuz

Meeting ID: 255 458 0251

**TAs:**

1. **Tahsin Alper Özkan (PhD) (**talper@sabanciuniv.edu )
2. **Cerin Ninan Kunnatharayil (PhD) (**cerinninan@sabanciuniv.edu)
3. **Erkut Gürol (MSc) (**erkutgurol@sabanciuniv.edu )

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| [**Electronic Circuits II - 20800 - EE 202 - 0**](https://suis.sabanciuniv.edu/prod/bwckctlg.p_disp_listcrse?term_in=202102&subj_in=EE&crse_in=202&schd_in=L) |
| **Type** | **Time** | **Days** | **Where** |
| Class | 11:40 am - 1:30 pm | M | FENS L045FENS L045 |
| Class | 11:40 am - 12:30 pm | W |

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| [**Electronic Circuits II Recit. - 20802 - EE 202R - A**](https://suis.sabanciuniv.edu/prod/bwckctlg.p_disp_listcrse?term_in=202102&subj_in=EE&crse_in=202R&schd_in=R) |
| **Type** | **Time** | **Days** | **Where** |
| Class | 5:40 pm - 7:30 pm | W | FENS G032 |

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| [**Electronic Circuits II Recit. - 20804 - EE 202R - B**](https://suis.sabanciuniv.edu/prod/bwckctlg.p_disp_listcrse?term_in=202102&subj_in=EE&crse_in=202R&schd_in=R) |
| **Type** | **Time** | **Days** | **Where** |
| Class | 10:40 am - 12:30 pm | R | FENS G032 |

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| [**Electronic Circuits II Recit. - 20806 - EE 202R - C**](https://suis.sabanciuniv.edu/prod/bwckctlg.p_disp_listcrse?term_in=202102&subj_in=EE&crse_in=202R&schd_in=R) |
| **Type** | **Time** | **Days** | **Where** |
| Class | 5:40 pm - 7:30 pm | R | FENS G032 |

**Office Hours:**

**Course Instructor: Monday, 10:40-11:30 (**FENS 1044**)**

**TAs (Homework): Wednesday, 13:40-14:30 (FENS 1033**)

**TAs (Homework): Thursday, 13:40-14:30 (FENS 1033**)

**Prerequisites by Course:** ENS 203 (Circuit I)

**by Topic:** Basic circuit analysis including Ohm’s and Kirchhoff’s Laws,

loop and nodal analysis, Thevenin and Norton equivalents, Sinusoidal forcing functions, phasors, and impedance / admittance.

**Co-requisites:** EE 200, Electronics Circuit Implementation.

**Catalog Description:** PN diode/device structure, physical operation, current voltage characteristics, and DC operation of BJT/MOSFET transistors/devices, along with diode and Transistor Breakdown and Temperature Effects, are analyzed. BJT/MOSFET small signal operations and models, and applying these models in basic discrete amplifier designs/configurations, along with different biasing concepts, are emphasized. Low-frequency response of BJT/MOSFET and CS-CE Amplifiers are studied. Internal capacitive effects and high frequency model of the BJT/MOSFET, along with high-frequency response of the CS-CE amplifiers, CG-CB, CD (Source follower)-CC (Emitter follower), Cascade and Cascode amplifiers are studied. Other wide band amplifier configurations, multistage amplifier examples, along with the BJT/MOSFET differential amplifiers are covered. Finally, the general feedback structure, some properties of negative feedback, and basic feedback circuit topologies are studied.

**Course Outcomes:**

*A student who successfully fulfills the course requirements will have demonstrated:*

1. Ability to analyze physical operation, current voltage characteristics, and DC operation/biasing of PN diode/device and BJT/MOSFET devices/transistors/structures,
2. Ability to analyze and understand electrical breakdown mechanisms and temperature effects of PN diode and BJT/MOSFET transistors,
3. Ability to understand small-signal operation and models of BJT/MOSFET transistors and applying these models for the realization of basic discrete amplifier designs/configurations,
4. Ability to apply DC biasing concept to maximize the performance of discrete amplifier designs/configurations,
5. Understand and analyze the low/high-frequency response of BJT/MOSFET, including internal capacitance effects,
6. Ability to design and analyze MOSFET/BJT based different amplifier concepts, including CS-CE, CG-CB, CD-CC, Cascade and Cascode amplifier configurations,
7. Understand and analyze the stability of amplifier, feedback concepts (positive and negative) and basic feedback topologies.

Implementation:

Classroom concepts are reinforced through recitations, implementing design exercises and homework problems.

Two in-class exams and one final exam will be implemented. It is in your best interest to attend all exams on the date of their delivery. Conflicts must be stated before the fact. Failure to attend an exam or to make previous arrangements results in a score of zero.

Incompletes are not given out as course grades as a consequence of missing an exam or homework assignment. Examinations are closed-book, closed-notes, and closed homework. Single sheets of summary equations are, however, permitted.

Textbooks:

1. Adel S. Sedra, Kenneth C. Smith, Microelectronic Circuits, 7th Edition, Oxford University Press, 2015 (www.sedrasmith.com)
2. Can be purchased through:

<https://www.homerbooks.com/urun/microelectronic-circuits>

Reference Books (available at the Information Center):

1. **B. Razavi, Fundamentals of Microelectronics, Wiley-2008**
2. **R. C. Jaeger, Microelectronic Circuit Design. New York: McGraw-Hill, 1997**.
3. R. T. Howe and C. G. Sodini, Microelectronics, Prentice Hall
4. **D. A. Neamen, Electronic Circuit Analysis and Design, New York: McGraw-Hill, 1996**
5. M. N. Hornstein, Microelectronic circuits and devices
6. **SPICE, Gordon Roberts and Adel Sedra, Second Edition, 1996**

Homework (**Total of 10 assigned last year!!**):

Homework will consist of problems given out on a weekly basis, nominally on Thursday’s. You are encouraged to work together on the problems, but please ensure that the final work handed in is your own. Homework is due at the end of one week from the day it was handed out.

Late homework is not accepted under any circumstances, since solutions to the homework will be uploaded to EE 202 in SUCourse + immediately after the homework is handed in. Homework must be uploaded to SUCourse + in a .pdf format. The grading of homework (as well as the exams) will emphasize the method used to arrive at the answer rather than the numerical result itself. Hence, it is most important that your work be legible, organized, and understandable. In addition, computer output, e.g. from SPICE, must be properly annotated to explain and label its key features.

Lectures:

Lecture attendance strongly recommended since you are responsible for any material covered in class.

Calculators:

An electronic hand calculator is necessary for both the exams and homework in this class. A programmable calculator or one that offers an equation “solver” function is not required, but strongly recommended. Students are responsible for knowing how to use their own calculators.

Computers and Software:

This class will also involve computer simulation of circuits using PSPICE. This program will be available on the course web-site for downloading or you obtain the same PSPICE student version software from the OrCAD website: http://www.orcad.com. Be sure to use PSpice 9.1 student edition. This includes PSpice A/D, Capture, Schematics, and PSpice Optimizer. Only PSpice A/D and Capture will be used in this course.

**Grading:**

2-Midterms : 55 % (25% + 30%)
Homework + Quiz : 5 % + 15%
Final : 25 %

**Top 5-Ways to Avoid an “A” Grade**

1. Skip lectures
2. Don’t put adequate effort into HW assignments
	1. Do it at the last minute
	2. Rely too much on collaboration
3. Don’t attend discussion/recitation sections
4. Don’t turn in HWs
5. Don’t review HW solutions, lecture notes and additional work/study problems

**EE 202 - Circuits II**

 **Course Outline**

**Semiconductors (1 Week)**

Chapter 3: (Page No: 134 – 167)

3.1 Intrinsic Semiconductors

3.2 Doped Semiconductors

3.3 Current Flow in Semiconductors

3.4 The p-n Junction

3.5 The p-n Junction with an Applied Voltage

3.6 Capacitive Effects in the p-n Junction

**Bipolar Junction Transistors BJTs (2.5 Weeks)**

Chapter 6: (Page No: 304 – 351)

6.1 Device Structure and Physical Operation

6.2 Current Voltage Characteristics

6.3 BJT Circuits at DC

**BJT in Amplifier Design (2 Weeks)**

Chapter 7:

7.1.1 Applying the BJT in Amplifier Design (Page No: 368 – 369)

7.2.2 Small Signal Operation and Models (Page No: 399 – 420)

7.3 Basic BJT Amplifier Configurations (Page No: 423 – 454)

7.4.2 Biasing in BJT Amplifier Circuits (Page No: 461 – 466)

7.5 Discrete Circuit BJT Amplifiers (Page No: 467 – 478)

6.4 Transistor Breakdown and Temperature Effects (Page No: 351 – 354)

**Midterm I (April 9/10th, April 16/17th Sat/Sun)**

**Frequency Response of BJT (2 Weeks)**

Chapter 10:

10.1 Low-frequency Response of the CS-CE Amplifiers (Page No: 699 – 710)

10.2.2 Internal Capacitive Effects and High Frequency Model of the BJT (Page No: 717 – 722)

10.3 High-frequency response of the CS-CE amplifiers (Page No: 722 – 738)

10.4Useful tools for the analysis of the high frequency response of amplifiers (Page No: 739 – 747)

10.6 High Frequency Response of the Source and Emitter Followers (Page No: 760 – 767)

10.8 Other Wide Band Configurations (Page No: 778 – 788)

**MOS Field-Effect Transistors (1 Week)**

Chapter 5: (Page No: 247 – 287)

5.1 Device Structure and physical operation

5.2 Current Voltage Characteristics

5.3 MOSFET Circuits at DC

**Small Signal Operation of MOSFETs (1.5 Weeks)**

Chapter 7:

7.2.1 Small Signal Operation and Models (Page No: 383 – 398)

7.3 Basic MOSFET Amplifier Configurations (Page No: 423 – 454)

7.4.1 Biasing in MOS Amplifier Circuits (Page No: 455 – 460)

7.5 Discrete-Circuit MOS Amplifiers (Page No: 467 – 478)

**Frequency Response of MOSFETs (1 Weeks)**

Chapter 10:

10.1 Low Frequency Response of the CS CE Amplifiers (Page No: 699 – 710)

10.2.1 Internal Capacitive Effects and High Frequency Model of the MOSFET and the BJT (Page No: 711– 716)

10.3 High Frequency Response of the CS CE Amplifiers (Page No: 722 – 739)

10.5 High Frequency Response of CG and Cascode Amplifiers (Page No: 748 – 760)

10.6 High Frequency Response of the Source and Emitter Followers (Page No: 760 – 767)

10.8 Other Wideband Amplifier Configurations (Page No: 778 – 787)

9.6.1 Multistage Amplifier Examples (Page No: 659 – 663)

**Midterm II – (May 28/29th)**

**Differential BJT Pair (1 Weeks)**

Chapter 9:

9.2 The BJT Differential Pair (Page No: 614 – 627)

**Feedback (1 Week)**

Chapter 11: (Page No: 808 – 828)

11.1 The General Feedback Structure

11.2 Some Properties of Negative Feedback

11.3 The Four Basic Feedback Topologies

LAST DAY OF CLASSES 14th Week

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